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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): YOR920030406US1 (8728-649)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on March 13, 2006

Signature _____

Typed or printed name Nathaniel T. Wallace

Application Number	Filed
10/733,210	December 10, 2003

First Named Inventor: Robert John Allen

Art Unit	Examiner
2825	Dinh, Paul

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 48,909
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

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March13, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Patent Application

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	Allen et al.	DOCKET: YOR920030406US1 (8728-649)
SERIAL NO:	10/733,210	GROUP ART UNIT: 2825
FILED:	December 10, 2003	EXAMINER: Dinh, Paul
FOR:	**FRAMEWORK FOR HIERARCHICAL VLSI DESIGN**	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Examiner:

In response to the Advisory Action dated February 2, 2006, Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal and a Pre-Appeal Brief Request For Review Form (PTO/SB/33).

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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Dated: March 13, 2006

Melithza Rodriguez

REMARKS

Please consider the following reasons for this Pre-Appeal Brief Request For Review.

Claims 1-12 and 16-30 are pending and stand rejected in the above-referenced application. Reconsideration of the rejection is respectfully requested in view of the remarks.

Claims 1, 16, and 28 are the pending independent claims. Only objections and rejections pertinent to Claims 1, 16, and 28 are addressed here.

Claims 1, 16, and 28 have been objected, wherein the Examiner suggested that the phrase "outputting a transformed hierarchical VLSI design" is not clearly described in the specification.

Respectfully, outputting a transformed hierarchical VLSI design is described at, among other places, page 6, lines 3-6, and page 45 lines 18-20. Further, an illustrative example is given at page 7, line 20 to page 8, lines 3, for example, "the isomorphism of the processed hierarchical graph is performed 309 and the processed hierarchical graph is stored in a corresponding database." Given the foregoing exemplary portions of the disclosure, Claims 1, 16, and 28 are believed to have clear support in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description as required under 37 C.F.R. 1.75. Reconsideration of the objection is respectfully requested.

Claim 28 has been objected to wherein the Examiner suggested that the phrase "a more operation, a split operation or a merge operation" is an incomplete claim structure as the object of the operations is not claimed.

Claim 28 claims, *inter alia*, "representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects; specifying a transformation behavior

applied to the design objects; processing the graph top-down beginning with a root cell of the graph to perform the transformation behavior on the hierarchical very large scale integrated design, wherein the transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design."

It is clear from Claim 28 that a structure of the hierarchical very large scale integrated design is represented as a graph comprising design objects, and that the graph is processed by performing a move operation, a split operation or a merge operation. Thus, the move, split and merge operations are performed on the graph representing the hierarchical very large scale integrated design. The Examiner's reconsideration of the objection is respectfully requested.

Claims 1-12 and 16-30 have been rejected under 35 U.S.C. 102(b) as being anticipated by Russell et al. (U.S. Patent No. 5,519,628). The Examiner stated essentially that Russell teaches all the limitations of Claims 1-12 and 16-30.

Claims 1 and 16 claim, *inter alia*, "specifying a transformation behavior applied to the design objects; processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design." Claim 28 claims, *inter alia*, "specifying a transformation behavior applied to the design objects; processing the graph top-down beginning with a root cell of the graph to perform the transformation behavior on the hierarchical very large scale integrated design, wherein the transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design."

Russell teaches methods for VLSI circuit design checking (see col. 6, liens 26-37). Russell does not teach, "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in Claims 1 and 16 and essentially as claimed in Claim 28. Russell teaches a top-down search in building a list of shape instances (LISA) (see col. 22, lines 14-28). Russel's top-down search for shape instances does not perform a transformation behavior, essentially as claimed in Claims 1, 16, and 28; the building of a LISA has no effect on the subject hierarchical very large scale integrated design and is a process for merely determining information from the hierarchical very large scale integrated design. Further, according to Russell, processing (building of the LISA) occurs in a bottom-up method. For example, see Figures 55 and 56 wherein after a search has been performed at 5502, a graph is modified, e.g., deleting a subgraph, by traversing an ancestor path 5628 (see col. 31 lines 39-41 and col. 32 lines 4-8). Traversing the ancestor path is a bottom-up processing beginning with leaf nodes. Russell does not teach, "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in Claims 1 and 16 and essentially as claimed in Claim 28. Therefore, Russell fails to teach all the limitations of Claims 1, 16, and 28.

In view of the above, Applicant's believe there is clear error in the rejection of Claims 1, 16, and 28 in view of Russell. Therefore, reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the present application, including Claims 1-12 and 16-30, is believed to be in condition for allowance. Early and favorable action is respectfully urged.

Respectfully submitted,

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